Remarks

The Official Action rejected claims 1-22. Applicant has amended claims 2, 3, 7, 8, 9, 14, 19, and 20. Reconsideration and allowance of the pending claims are respectfully requested.

Claim Rejections under 35 USC 112

The Office Action rejected claim 14 due to lack of antecedent basis for element "the memory" in the last paragraph. Applicant has amended element of "memory" in the second paragraph and other parts of the claim into "external memory", in order to meet the antecedent basis requirement. Applicant respectfully requests reconsideration and withdrawal of the present rejection.

Claim Rejections under 35 USC 102

The Official Action rejected claims 1-4, 7-12, 14-16 and 19-21 under 35 USC 102(e) as being anticipated by Chatterjee et al. (US 2005/01829906). Applicant respectfully requests reconsideration and withdrawal of the present rejection.

As is well-established, in order to successfully assert a prima facie case of anticipation, the Office Action must provide a single prior art document that includes every element and limitation of the claim or claims being rejected. Therefore, if even one element or limitation is missing from the cited document, the Office Action has not succeeded in making a prima facie case.

Claims 1-4 and 7-8 rejections

Each of claims 1-4 and 7-8 recites a method of a network processor comprising a plurality of microengines that process network packets, the method comprising: updating an entry in a memory external to the network processor; identifying a microengine of the plurality of microengines that has stored the entry in a local memory for the microengine; and writing information to a buffer for the identified microengine that indicates the entry has been updated, which is unanticipated by Chatterjee.

Chatterjee teaches a method of maintaining cache coherency between a first controller and a peer controller, wherein each of the controllers may include a processor (paragraph 0034). The method of Chatterjee is co-operated by the two controllers, for example, the first controller receives from a host device a write request to write data to a logical driver (160-166) external to the first controller, stores the data in its cache memory, post the cached data to the logical driver (160-166) external to the first controller, writes the header information related to a cache line storing the data to a buffer within the first controller, transmit the header information and associated data to the peer controller so that the peer controller can update its mirror cache memory to maintain cache coherency between the two controllers (Fig. 1 and corresponding descriptions).

There is nothing from Chatterjee that shows a structure of the processor in the controller, no to say, the processor comprising a plurality of microengines. Thus, there is nothing from Chatterjee that teaches identifying a microengine, and writing the information to the buffer for the identified microengine. Secondly, Chatterjee teaches the cache coherency method between two controllers each having a processor, but not a method within a same processor as required by claims 1-4 and 7-8.

Thirdly, the Office Action regards the cache memory in the first controller as the memory external to the processor of claims 1-4 and 7-8, and the mirrored cache memory of

the peer controller as the local memory of the microengine. Applicant is confused about which of the processors of the first controller and the peer controller is regarded as the processor of claims 1-4 and 7-8, since neither of the processors has the mirrored cache memory as its local memory. Claims 1-4 and 7-8 teaches a method of updating an entry in a memory external to the processor and then updating a local memory inside of the processor. However, Chatterjee teaches updating the memory (cache memory of the first controller) external to the processor of the first controller, and mirroring the update to another memory (mirror cache memory of the peer controller) external to the processor of the peer controller.

Since Chatterjee does not teach each and every limitation of claims 1-4 and 7-8, Chatterjee does not anticipate the invention of claims 1-4 and 7-8. Applicant respectfully requests the rejection of claims 1-4 and 7-8 be withdrawn.

Moreover, Applicant would like to point out that **claim 2** which recites reading the entry from the memory external to the network processor to update the local memory for the microengine in response to determining, based upon the information written to the buffer, that the entry has been updated, is unanticipated by Chatterjee.

As stated above, Chatterjee teaches the method between two controllers each having a processor, while method of claims 1-4 and 7-8 is performed by the same processor. In other words, Chatterjee teaches that updating the external logical driver and writing information to the buffer are operated by the first controller and updating the mirror cache memory based upon the buffered information is operated by the peer controller, while they are operated by the same processor according to claims 1-4 and 7-8.

Moreover, although Chatterjee discloses in paragraph 12 that the buffered information and associated data are transmitted for the peer controller to update its mirrored memory, Chatterjee does not clarify where the associated data is. However, in many of other parts of Chatterjee clearly mention that the associated data is within the buffer of the first controller,

see paragraph 0047 about update meta-data, paragraph 0018 and third paragraph of claim 7. In light of this, Chatterjee teaches reading the associated data from the buffer to update the mirror memory of the peer controller, rather than reading the entry from the memory external to the processor to update the mirror cache memory of the peer controller, as required by claim 2.

Further, Applicant would like to point out that **claim 3** recites the information is written into a scratch ring of the buffer, is unanticipated by Chatterjee.

Although Chatterjee discloses the header structure in Fig. 2 and its corresponding description, Chatterjee says nothing about in what buffer structure that the header is stored, not to say, in the scratch ring of the buffer. Chatterjee discloses that the first controller transmits the header information to the peer controller if any header information is added to the buffer (paragraph 0082), however, Chatterjee does not teach how to detect if any information is added into the buffer in details, no to say, detecting with the use of the scratch ring structure of the buffer, which may be one purpose of using the scratch ring in the present application. In view of this, Chatterjee does not anticipate that the information is written into a scratch ring of the buffer, as required by claims 1-4 and 7-8.

In addition. Applicant would like to point out that **claim 7** which recites the information further indicates that all entries in the local memory for the microengine are invalid, if more than a threshold number of entries of the memory external to the network processor are updated, is unanticipated by Chatterjee.

Chatterjee teaches after the data is written to the cache memory in the first controller, the first controller writes header information related to affected cache lines to the buffer, and writes data to the logical driver, meanwhile the data change is mirrored in the peer controller. However, Chatterjee does not teach how the header information will be if more that a threshold number of cache lines are updated.

Claims 9-12, 14-16 and 19-21 rejections

For similar reasons proffered for claims 1-4 and 7-8, claims 9-12, 14-16 and 19-21 is unanticipated by Chatterjee.

Claim Rejections under 35 USC 103 (Chatterjee/Joy)

The Official Action rejected claims 5, 6, 13, 17, 18 and 22 under 35 USC 103(a) as being unpatentable over Chatterjee in further view of Joy (US Patent 2002/0138717).

Claims 5, 6, 13, 17, 18 and 22 include one of claims 1, 9, 14 and 19 as a base claim. Therefore, claims 5, 6, 13, 17, 18 and 22 are allowable for the similar reason proffered for claims 1, 9, 14 and 19. Applicant respectfully requests reconsideration and withdrawal of the present rejection.

Conclusion

The foregoing is submitted as a full and complete response to the Official Action. Applicant submits that all remaining claims are in condition for allowance. Reconsideration is requested, and allowance of all remaining claims is earnestly solicited.

Should it be determined that an additional fee is due under 37 CFR §§1.16 or 1.17, or any excess fee has been received, please charge that fee or credit the amount of overcharge to deposit account #02-2666. If the Examiner believes that there are any informalities which can be corrected by an Examiner's amendment, a telephone call to the undersigned at (503) 439-8778 is respectfully solicited.

Respectfully submitted,

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